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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,815	12/08/2003	Bruce M. Gilbert	BEA920020006US1	7578

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EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,815	GILBERT ET AL.	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-19 have been examined.

Claims 1-19 have been rejected.

Claim Objections

1. Claim 14 is stated as being dependent on claim 16 but it seems more likely that Claim 14 should be dependent on claim 13, while claims 15, 16 and 17 are dependent on claim 14 because they state limitations "the normal mode", "the correction mode" and "the restart mode" which are introduced in claim 14 and would otherwise lack antecedent basis in each claim. To cover all grounds of objection, claims 15-17 are additionally objected to for containing the above cited antecedence problems.

Claim 19, the second to last line should read "are processed and *including* logic to detect".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 13-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitamura (US Patent 4,701,915).

3. As per claim 1, Kitamura ('915) discloses a method comprising:

detecting a correctable error while processing a transaction within a pipeline (column 4 lines 54-56);

outputting the transaction from the pipeline into an error queue (the data register 12 of Figure 1 and column 5 lines 12-15);

processing a correction command within the pipeline to correct the correctable error within the transaction (column 5 lines 12-17); and,

reprocessing the transaction within the pipeline, where the correctable error therewithin has been corrected (column 5 lines 17-21).

3. As per claim 2, Kitamura ('915) discloses the method of claim 1, further comprising, prior to processing the correction command, inputting the correction command into the pipeline (column 2 lines 34-40, the re-writing command).

4. As per claim3, Kitamura ('915) discloses the method of claim 2, further comprising, prior to inputting the correction command into the pipeline, operating the pipeline in a correction mode (column 4 line 67 through column 5 line 2, the pausing of data in the pipeline indicates a correction mode).

5. As per claim 4, Kitamura ('915) discloses the method of claim 1, further comprising, prior to reprocessing the transaction within the pipeline, inputting the

transaction from the error queue back into the pipeline (column 5 lines 15-17, rewrites corrected instruction into memory before re-executing).

6. As per claim 5, Kitamura ('915) discloses the method of claim 4, further comprising, prior to inputting the transaction from the error queue back into the pipeline, operating the pipeline in a restart mode (column 1 lines 52-53).

7. As per claim 6, Kitamura ('915) discloses the method of claim 1, further comprising, after reprocessing the transaction within the pipeline, operating the pipeline in a normal mode (column 1 lines 7-8, the term error recovery implies a recovery to a normal pre-error pipeline operation), as shown in Figure 3 and 5).

8. As per claim 13, Kitamura ('915) discloses a controller for a node of a system comprising:

a pipeline in which transactions are processed (as shown in Figure 2);

a mode controller to control a mode in which the pipeline operates (Figure 2, element 15); and,

an error queue to which those of the transactions including correctable errors are routed for correction of the correctable errors and reprocessing of the transactions (column 5 lines 12-15, the data register).

9. As per claim 14, Kitamura ('915) discloses the controller of claim 16, wherein the mode in which the pipeline operates includes one of a normal mode (as shown in Figure 3), a correction mode, or a restart mode.

10. As per claim 15, Kitamura ('915) discloses the controller of claim 13, wherein the mode controller switches the operation of the pipeline in the normal mode for processing those of the transactions not including the correctable errors (as shown in Figure 3, and when an error is detected additional actions are performed as described in column 2 lines 35-36 and indicated by the pipeline stall in Figure 5).

11. As per claim 16, Kitamura ('915) discloses the controller of claim 13, wherein the mode controller switches the operation of the pipeline in the correction mode for correcting the correctable errors within those of the transactions including the correctable errors (column 2 lines 35-36).

12. As per claim 17, Kitamura ('915) discloses the controller of claim 13, wherein the mode controller switches the operation of the pipeline in the restart mode for processing those of the transactions including the correctable errors after the correctable errors have been corrected (column 2 lines 52-54).

13. As per claim 18, this claim recites limitations found in claim 14 (assuming its dependence on claim 13, as noted in the objection to claim 14, above) and is rejected on the same grounds as claim 14.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 7-~~18~~ 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura ('915) in view of Weber (US Patent 6,631,448).

15. As per claim 7, Kitamura ('915) discloses a system comprising: at least one controller to process transactions relating to a local RAM of a node (column 4 line 4), including correcting correctable errors within the transactions in a non-inline manner in a separate correction mode (as shown in Figure 5, the pipeline is halted while correcting errors. Also see column 2 lines 51-54).

Kitamura ('915) does not expressly disclose the system comprising:

a plurality of nodes interconnected to one another, each node comprising:

a plurality of processors; and

local random-access memory (RAM) for the plurality of processors.

Weber ('448) teaches a system wherein multiple nodes are connected, each with multiple processors and a shared memory (as shown in Figure 4).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the transaction correction system disclosed by Kitamura ('915) such that it is implemented in the multi-node multi-processor system taught by Weber ('448). This modification would have been obvious because it allows for increased processing power (Weber ('448) column 2 lines 25-32) while multiple nodes allows for a physically distributed system (Weber ('448) column 5 lines 7-10).

16. As per claim 8, Kitamura ('915) in view of Weber ('448) discloses the system of claim 7, wherein each controller comprises a pipeline in which the transactions are processed and that includes logic to detect the correctable errors within the transactions (Kitamura ('915) column 4 lines 6-12).

17. As per claim 9, Kitamura ('915) in view of Weber ('448) discloses the system of claim 7, wherein each controller comprises a mode controller to control a current mode in which the controller is operating (Kitamura ('915) Figure 1 element 15).

18. As per claim 10, Kitamura ('915) in view of Weber ('448) discloses the system of claim 7, wherein each controller comprises an error queue to which those of the transactions including the correctable errors are routed for correction and reprocessing (Kitamura ('915) column 5 lines 12-15, the data register).

19. As per claim 11, Kitamura ('915) in view of Weber ('448) discloses the system of claim 7, wherein each controller includes a normal mode in which the transactions are processed (as shown in Kitamura ('915) Figure 3) and a restart mode in which those of the transaction including the correctable errors are reprocessed after correction of the correctable errors (Kitamura ('915) column 5 lines 17-21).

19. As per claim 12, Kitamura ('915) in view of Weber ('448) discloses the system of claim 7, wherein each controller of each node comprises an application-specific integrated circuit (ASIC) (Kitamura ('915) Figure 1 shows multiple application-specific circuits such as a decoder 13, error detection and correction circuit 14 and pipeline controller 15).

20. As per claim 19, this claim recites limitations found in claim 8 and is rejected on the same grounds as claim 8.

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Brown ('160), Zumkehr ('118), Suzuki ('891), Nakase ('577), Lee('860) and Jamil ('028) teach systems that perform error correction and detection within a pipeline; Manton ('750) teaches a system that calculates and stores ECC data as part of a pipeline, Sato ('103) teaches a system that detects and marks erroneous instructions, DeSota ('665) teaches a pipeline hazard detection system with transaction routing for reprocessing.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER